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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/577,863	04/28/2006	Masamichi Ishihara	SAK-5286	2248

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EXAMINER	
HARRISTON, WILLIAM A	
ART UNIT	PAPER NUMBER
2826	
MAIL DATE	DELIVERY MODE
03/10/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/577,863	ISHIHARA, MASAMICHI	
	Examiner	Art Unit	
	WILLIAM HARRISTON	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) *24-46* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 April 2006* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/5/2007, 4/28/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-23 in the reply filed on 1/12/2009 is acknowledged.

Priority

2. Applicant's claim for the benefit of a prior-filed application is acknowledged.

Information Disclosure Statement

3. The information disclosure statements filed on 10/5/2007 and 4/28/2006 have been considered.

Oath/Declaration

4. The oath or declaration filed on 4/28/2006 is acceptable.

Drawings

5. The drawings filed on 4/28/2006 are acceptable.

Specification

6. The abstract of the disclosure and the specification filed on 4/28/2006 are acceptable.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-7, 10-15, and 17-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Tanida et al. (US 2006/0038300 A1 hereinafter Tanida).

9. Regarding claim 1, figures 4 and 7 of Tanida disclose a semiconductor device consisting of a first semiconductor device (41) having outside electrode terminals (45a) on its lower surface, a second semiconductor device (41) electrically connected with said first semiconductor device and secured on said first semiconductor device, characterized in that:

said first semiconductor device (41) has:

a semiconductor substrate (2);

a multilayer wiring part (11) including a plurality of circuit elements (3) formed at a first main surface side of said semiconductor substrate and wiring connected with said circuit elements;

a first insulating layer (13) for covering said multilayer wiring part;

a second insulating layer (16) for covering a second main surface to become an opposite face against the first main surface of said semiconductor substrate;

a plurality of post electrodes (12) formed on respective specified wiring of said multilayer wiring part to be exposed in a surface of said first insulating layer;

a plurality of through-type electrodes (45) provided to pierce through said semiconductor substrate (2) and said second insulating layer (16) from specified depth of said multilayer wiring part (11), brought into contact to said semiconductor substrate (2) through an insulating film (42) and connected with specified wiring of said multilayer wiring part respectively; and

said outside electrode terminals (45a) connected to said through-type electrodes (45);

said second semiconductor device (41) has:

a semiconductor substrate (2);

a multilayer wiring part (11) including a plurality of circuit elements (3) formed at a first main surface side of said semiconductor substrate and wiring (11) connected with said circuit elements;

a first insulating layer (13) for covering said multilayer

wiring part;

a second insulating layer (16) for covering a second main surface to become an opposite face against the first main surface of said semiconductor substrate;

at least post electrodes (12) formed on respective specified wiring of said multi layer wiring part (11) to be exposed in a surface of said first insulating layer, and in said first semiconductor device, said post electrodes (12) come in a lower surface and said post electrodes in the lower surface are provided with said outside electrode terminals (10a); (See paragraph [0149])

said post electrodes in the lower surface of said second semiconductor device are electrically connected with said through-type electrodes in the upper surface of said first semiconductor device through joints.

FIG. 4

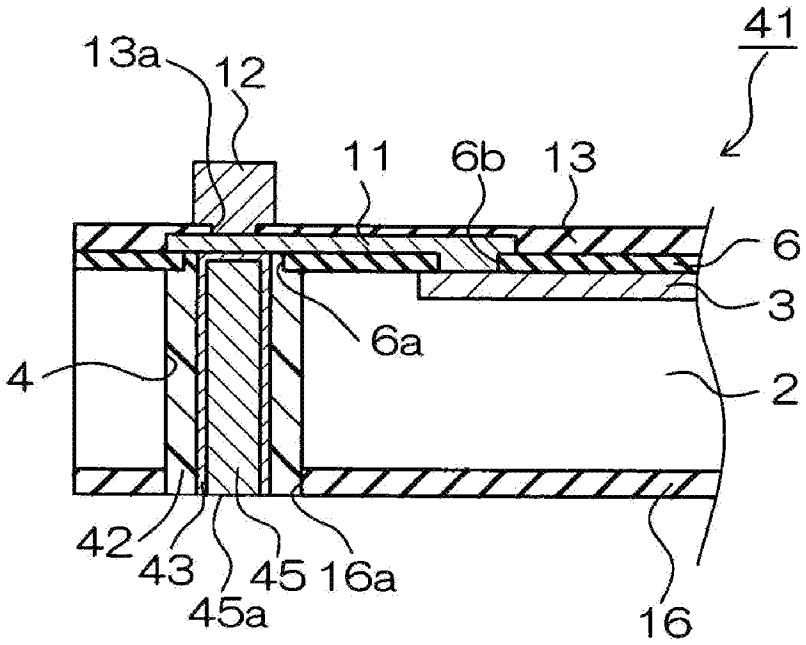

FIG. 7

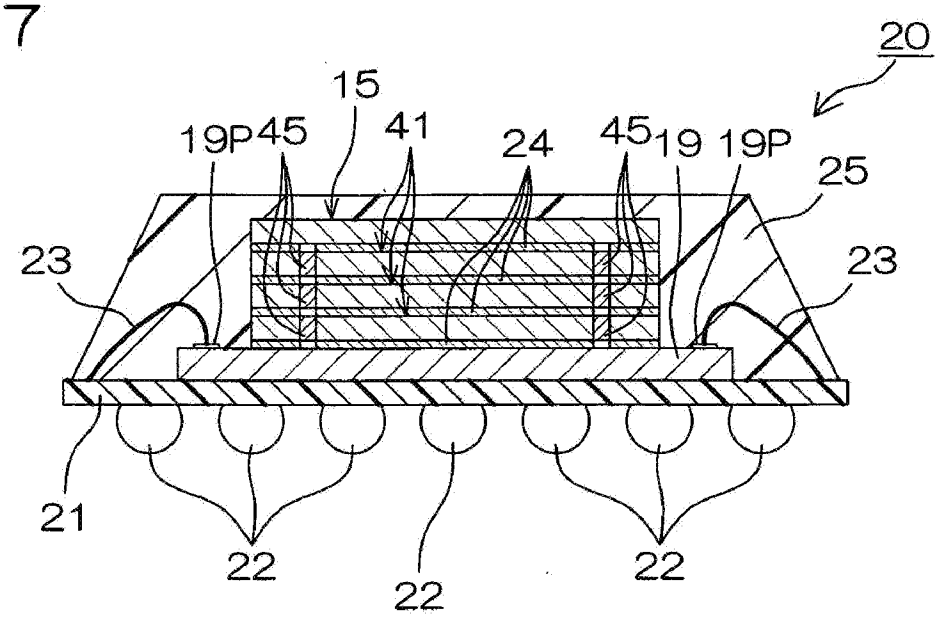

Figure 7 discloses a stack of three semiconductor devices (41) which are shown in detail in figure 4 and a device (15) on top of this stack. To clarify, Examiner has

interpreted the first semiconductor device to be the device (41) on the bottom of the stack shown in figure 7. Examiner has interpreted the second semiconductor device to be the device (41) beneath semiconductor chip (15) as shown in figure 7.

10. Regarding claim 2, Tanida discloses the device of claim 1 for the reasons stated above. Tanida further discloses:

a third semiconductor device (41) stacked and secured between said first semiconductor device (41) and said second semiconductor device (41) over one to a plurality of steps, characterized in that:

said third semiconductor device has:

a semiconductor substrate (2);

multilayer wiring part (11) including a plurality of circuit elements (3) formed at a first main surface side of said semiconductor substrate and wiring connected with said circuit elements;

a first insulating layer (13) for covering said multilayer wiring part (11);

a second insulating layer (16) for covering a second main surface to become an opposite face against the first main surface of said semiconductor substrate;

a plurality of post electrodes (12) formed on respective specified wiring of said multilayer wiring part to be exposed in a surface of said first insulating layer;

a plurality of through-type electrodes (45) provided to pierce through said semiconductor substrate and said second insulating layer from specified depth of said multilayer wiring part, brought into contact to said semiconductor substrate through an insulating film (43) and connected with specified wiring of said multilayer wiring part respectively, and

the post electrodes (12) on the upper/lower surfaces of said third semiconductor device are electrically connected with the post electrodes or through-type electrodes of the semiconductor device at the upper stage side and the semiconductor device at the lower stage side through joints.

11. Regarding claim 3, Tanida discloses the device of claim 1 for the reasons stated above. Tanida further discloses the device characterized in that said semiconductor devices (41, 41, 41) at the respective stages will become a single body (20) and the respective semiconductor devices overlap each other in corresponding fashion in a same size.

12. Regarding claim 5, Tanida discloses the device of claim 1 for the reasons stated above. Tanida further discloses the device is characterized in that the respective post electrodes (12) on the upper surface of said first semiconductor device (41) and the respective through-type electrodes (45) on the lower surface of said second

semiconductor device are brought into correspondence and are electrically connected respectively through said joints. See paragraph [0149].

13. Regarding claim 6, Tanida discloses the device of claim 1 for the reasons stated above. Tanida further discloses the device characterized in that said joints are not used for joining the respective through-type electrodes (45) on the upper surface of said first semiconductor device (41) with the respective through-type electrodes (45) on the lower surface of said second semiconductor device (41) but, said post electrodes (12) engaged in said joining of said one semiconductor device (41) protrude and these protruding portions are connected to said through -type electrodes of the facing semiconductor device (41) with metal joining.

14. Regarding claim 7, Tanida discloses the device of claim 1 for the reasons stated above. Tanida further discloses the device wherein said post electrodes (12) are formed of stud bump electrodes. See paragraph [0122] and [0091].

15. Regarding claim 10, Tanida discloses the device of claim 1 for the reasons stated above. Tanida further discloses the device characterized in that out of said first and second semiconductor devices said semiconductor substrate of one semiconductor device is a silicon substrate. See paragraph [0089].

Regarding the limitation “wherein the semiconductor substrate of the other semiconductor device is a compound semiconductor device.”, the applicant is respectfully advised that in considering the disclosure of a reference, it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom.” *In re Preda*,

159 USPQ 342 (CCPA 1968). In this case, it would have been obvious to one of ordinary skill in the art to form the semiconductor substrate of the other semiconductor device from a compound semiconductor material, since one of ordinary skill would have recognized such a semiconductor material as being one of the many materials available in the prior art for forming a substrate, selection of a specific one over another being an obvious matter of meeting the specific requirements of a given application.

16. Regarding claim 11, Tanida discloses the device of claim 1 for the reasons stated above. Tanida further discloses wherein the through type electrodes and the post electrodes are formed from copper. See paragraph [0158].

17. Regarding claim 12, Tanida discloses the device of claim 1for the reasons stated above. Tanida further discloses the device wherein the gap between said first semiconductor device (41) and said second semiconductor device (41) is filled with insulating resin (24). Applicant discloses at paragraph [0032] that the insulating resin can be formed from epoxy. Paragraph [0162] of Tanida discloses the gap between semiconductor chips is filled with epoxy resin.

18. Regarding claim 13, Tanida discloses the device of claim 1 for the reasons stated above. Figure 8 of Tanida further discloses the device wherein first and second semiconductor devices (60) have a plurality of post electrodes (62) exposed in a first surface of said first insulating layer (13), and through-type electrodes (10) are formed at exposed ends of specified said post electrodes.

19. Regarding claim 14, Tanida discloses the device of claim 1 for the reasons stated above. Tanida further discloses wherein the post electrodes (12) are larger than said through -type electrodes (45) in diameter.

20. Regarding claim 15, Tanida discloses the device of clam 1 for the reasons stated above. Tanida further discloses wherein said circuit elements (3) are active elements and passive elements. See paragraph [0088].

21. Regarding claim 17, figure 4 of Tanida discloses:

a semiconductor device characterized by having:

a semiconductor substrate (2);

a multilayer wiring part (11) including a plurality of circuit elements (3) formed at a first main surface side of said semiconductor substrate and wiring connected with said circuit elements;

a first insulating layer (13) for covering said multi layer wiring part;

a second insulating layer (16) for covering a second main surface to become an opposite face against the first main surface of said semiconductor substrate;

a plurality of post electrodes (12) formed on respective specified wiring of said multilayer wiring part to be exposed in a surface of said first insulating layer;

a plurality of through-type electrodes (45) provided to pierce through said semiconductor substrate and said second insulating layer from a specified depth of said multilayer wiring part, brought into contact to said semiconductor substrate through an insulating film (5) and connected with specified wiring of said multilayer wiring part respectively.

22. Regarding claim 18, Tanida discloses the device of claim 17 for the reasons state above. Tanida further discloses the device wherein protruding electrodes are formed at exposed ends of specified said post electrodes (12) and said through-type electrodes.

23. Regarding claim 19, Tanida discloses the device of claim 17 for the reasons stated above. Tanida further discloses said post electrodes (12) are larger in diameter tan said through-type electrodes (45).

24. Regarding claim 20, the method of forming a device is not germane to the issue of patentability of the device itself. Therefore this limitation has not been given patentable weight. Ex Parte Pfeiffer, 1962 C.D. 408 (1961).

25. Regarding claim 21, Tanida discloses the device of claim 17 for the reasons stated above. Tanida further discloses wherein the through type electrodes and the post electrodes are formed from copper. See paragraph [0158].

26. Regarding claim 22, Tanida discloses the device of clam 17 for the reasons stated above. Tanida further discloses wherein said circuit elements (3) are active elements and passive elements. See paragraph [0088].

Claim Rejections - 35 USC § 103

27. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

28. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

29. Claims 4, 16 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanida as applied to claims 1 and 17 above.

30. Regarding claim 4, Tanida discloses the device of claim 1 for the reasons stated above. Tanida discloses second semiconductor devices disposed and secured in parallel on said first semiconductor device. Tanida discloses the invention except for wherein pluralities of second semiconductor devices are smaller than the first semiconductor device. It would have been obvious an obvious matter of design choice to form smaller second semiconductor devices, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. St. Regis Paper Co. V. Bemis Co., 193 USPQ 8.

31. Regarding claims 16 and 23, Tanida discloses the devices of claims 1 and 17 for the reasons stated above. Tanida discloses the device except for a semiconductor substrate (2) having a thickness between 5 and 50 micrometers and the first insulating layer (13) having a thickness between 20 and 100 micrometers. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form

a substrate having a thickness between 5 and 50 micrometers and a first insulating layer having a thickness between 20 and 100 micrometers, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges requires only routine skill in the art. In re Aller, 105 USPQ 233.

32. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanida as applied to claim 1, taken with Murata.

33. Regarding claim 8, Tanida discloses the device of claim 1 for the reasons stated above. Tanida does not disclose a metal plate between first and second semiconductor devices.

However, figures 1a-2b of Murata do disclose a metal plate (10a) having insulating holes (18).

One having ordinary skill in the art would be motivated to provide a metal layer between first and second stacked semiconductor devices in order to improve the performance of a stacked device by ensuring adequate flatness and providing heat dispersion between adjacent devices.

Further, figure 2b of Murata taken with Tanida discloses in the portion of said insulating holes (element 18 of Murata), what would be said post electrodes on the upper surface of said first semiconductor device (element 12 of Tanida/element 28 of Murata) are electrically connected with said through-type electrodes (see paragraph [0112] of Murata) on the lower surface of said second semiconductor device (element 26 of Murata) through said joints in a state without contacting said metal plate (10a) ,

said through-type electrodes and said post electrodes of said first semiconductor device and said second semiconductor device to face said metal plate are electrically connected with said metal plate through said joints.

34. Regarding claim 9, Tanida taken with Murata disclose the device of claim 1 for the reasons sated above. However, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM HARRISTON whose telephone number is (571)270-3897. The examiner can normally be reached on Monday - Friday 9 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue A. Purvis can be reached on (571)272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/W. H./
Examiner, Art Unit 2826
/VICTOR A MANDALA JR/
Examiner, Art Unit 2826
3/9/09